AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method of interlinking first and second switch modules in a common switch node for use in a communications network where the common switch node is coupled to other switch nodes by one or more external links, comprising the steps of:

providing first and second redundant node-internal links between said first and second switch modules contained within the common switch node;

receiving a data packet with a destination address at the first switch module;

over-writing at the first switch module said destination address with a routing tag identifying only an active one of the first and second links; and

outputting from the first switch module the data packet only to said active one of said first and second links identified by the routing tag.

2. (Original) A method according to claim 1, further including the step of simultaneously receiving at first and second link terminals in said first switch module the data packet having the routing tag.

3. (Original) A method according to claim 1, further including the steps of:

passing the data packet through a switch core and therein performing the overwriting step.

4. (Original) A method according to claim 1, further including the steps of:

detecting a fault condition in the active one of said first and second links; and thereafter

the over-writing step overwrites said destination address with the routing tag identifying the other of said first and second links.

5. (Currently Amended) A module ~~in~~ within a switch node operatively ~~linked~~ linkable with a second module ~~in~~ within the same switch node, comprising:

first and second redundant node-internal links connecting the first module to the second module contained in the switch node; and

a routing tagger to receive a stream of data packets destined for the second module and to apply a node-internal routing tag to the data packets in the stream to direct the stream to only one of the first and second redundant links so that only the one link is used to rotate the data packets to the second module;

a set of device boards outputting the data packets with standard addresses;

a switch core in communication with the set of device boards to receive the data packets and overwrite the standard addresses with the node-internal routing tags;

first and second redundant link terminals in communication with the switch core;

the first link coupled to the first link terminal and to the second module, said first link associated with a first unique one of the routing tags; and

the second link coupled to the second link terminal and to the second module, said second link associated with a second unique one of the routing tags.

6. (Canceled).

7. (Currently Amended) A module according to claim ~~6~~ 5, wherein:

at least one of said first and/or second link terminals receive the data packets;

the first link terminal passes the data packets to the first link if the switch core overwrites the standard address with the first unique one of the routing tags; and

the second link terminal passes the data packets to the second link if the switch core overwrites the standard address with the second unique one of the routing tags.

8. (Original) A module as in claim 7, wherein both the first and second link terminals receive said data packets, and one of the first and second link terminals blocks the passage of said data packets to a corresponding one of the first and second links.

9. (Original) A module as in claim 7, wherein both the first and second link terminals receive said data packets, and one of the first and second link terminals also blocks the passage of said data packets to a corresponding one of the first and second links until the overwrite changes from a current one of the first and second routing tags to the other of the first and second routing tags.

10. (Original) A module according to claim 7, wherein:

said set of device boards create said data packets without regard to the redundancy of the first and second links.

11. (Original) A module according to claim 7, wherein:

said switch core overwrites the standard addresses with the first unique one of said routing tags under a first operational condition, and

said switch core overwrites the standard addresses with the second unique one of said routing tags under a second operational condition different from said first operational condition.

12. (Original) A module according to claim 11, wherein the first operational condition identifies a detected normal condition in the first link and the second operational condition identifies a detected fault condition in the first link.

13. (Currently Amended) A single switch node~~,~~ comprising within the physical boundaries of that node:

first and second switch modules operatively linked to each other within the single switch node, each module ~~having~~ containing:

a set of device boards for outputting data packets having standard routing tags;

a switch core in communication with the set of device boards to receive the data packets and overwrite the standard routing tags with modified routing tags;

first and second redundant link terminals in communication with the switch core;

a first node-internal link coupled to the first link terminal and to the other of said modules, said first link associated with a first unique one of said modified routing tags; and

a second node-internal link, redundant to the first link, coupled to the second link terminal and to the other of said modules, said second link associated with a second unique modified routing tag, wherein:

at least one of said first and second link terminals configured to receive said data packets, and wherein:

said first link terminal is configured to pass ~~passes~~ said data packets to the first link when the switch core overwrites said standard routing tag with said first unique one of said modified routing tags, and

said second link terminal is configured to pass ~~passes~~ said data packets to the second link when the switch core overwrites said standard routing tag with said second unique one of said modified routing tag.

14. (Original) A switch node according to claim 13, further including:

a third module between said first and second modules, comprising a space switching module.

15. (Original) A switch node according to claim 13, further including:

a plurality of modules between said first and second modules, each comprising a space switching module.

16. (Currently Amended) A ~~set of ATM~~ switch ~~modules~~ module for use in a ~~an ATM~~ switch node, ~~each~~ comprising:

a power distribution layer;

a clock ~~functions~~ function layer in communication with the power distribution layer;

~~ATM~~ switch planes in communication with the clock functions layer;

an interconnection links layer for connecting to another interconnection links layer of another of said set of ~~ATM~~ switch modules via at least first and second redundant links, said interconnection links layer for detecting faults in said links and redirecting communication to one of said first and second links whenever faults are detected in the other of said links; and

an applications layer in communication with the ~~interconnections~~ interconnection links and providing data packets to said interconnection links layer, said applications layer operating independently of said detecting and re-directing aspects of said interconnection links layer.

17. (Currently Amended) A switch node comprising:

a first switch module operatively communicating with a second switch module through a set of links,

said set of links including a first set of links actively carrying data packets between the first and second modules and at least one extra link that remains idle until a failure is detected in any one of the first set of links, whereupon the extra link takes the place of the failed link in carrying assigned ones of said data packets,

each switch module including:~~;~~

a power distribution layer;

a clock function layer in communication with the power distribution layer;

switch planes in communication with the clock function layer;

an interconnection links layer for connecting to another interconnection links layer of another of said set of switch modules via said set of links, said interconnection links layer for detecting the failure in said one link and redirecting communication from the failed link to the extra link; and

an applications layer in communication with the set of links and providing data packets to said interconnections links layer, said applications layer operating independently of said detecting and re-directing aspects of said interconnection links layer.

18. (Original) A switch node according to claim 17, including:

multiple extra links, each available to take the place of any failed ones of the first set of links in carrying assigned ones of the data packets.

19. (Currently Amended) A switch node according to claim 17, further including:

internal routing taggers to tag the data packets to particular ones of the ~~first~~ set of links until ~~any one of the first set of links~~ the one link fails whereupon said taggers instead tag the data packets otherwise destined for the failed link to the extra link.

20. (Currently Amended) A single switch node comprising:

a number N of first links and a number M of second links, all connecting first and second switch modules contained within physical boundaries of the single switch node, each of the first and second node-internal switch ~~module~~ modules including:

a fault detector to determine N number of currently operable ones of said N&M first and second links;

a switch core communicating between at least one device circuit and the first and second links to route data packets from the device circuits to at least the N number of currently operable first and second links; and

a device-side switch port interface between the device circuit and the switch core to add internal routing tags to the data packets identifying only the N number of currently operable first and second links; and

a link-side switch port interface between the switch core and the links to read the internal routing tags and route the data packets to the N number of currently operable first and second links.

21. (Original) A switch node according to claim 20, wherein:

N is one and M is one.

22. (Original) A switch node according to claim 20, wherein:

N is at least two and M is one.

23. (Original) A switch node according to claim 20, wherein:

N is at least two and M is at least two.

24. (Original) A switch node according to claim 20, further including:

N+M number of link exchanges coupled between the switch core and corresponding ones of the first and second links; and wherein:

the link-side switch port interface includes N+M link-side switch port interfaces, one per link exchange.

25. (Original) A switch node according to claim 20, wherein:

each switch module includes device circuits, and

the device-side switch port interface includes multiple device-side switch port interfaces, one per device circuit.

26. (New) A switch node according to claim 20, wherein each module includes:

a power distribution layer;

a clock function layer in communication with the power distribution layer;

switch planes in communication with the clock function layer;

an interconnection links layer for connecting to another interconnection links layer of another of said set of switch modules via said first and second links, said interconnection links layer for detecting faults in said links and redirecting communication to one of said first and second links whenever faults are detected in the other of said links; and

an applications layer in communication with the interconnection links and providing data packets to said interconnections links layer, said applications layer operating independently of said detecting and re-directing aspects of said interconnection links layer.

27. (New) A switch node according to claim 13, wherein each switch module includes:

a power distribution layer;

a clock function layer in communication with the power distribution layer;

switch planes in communication with the clock function layer;

an interconnection links layer for connecting to another interconnection links layer of another of said set of switch modules via said first and second links, said interconnection links layer for detecting faults in said links and redirecting communication to one of said first and second links whenever faults are detected in the other of said links; and

an applications layer in communication with the interconnection links and providing data packets to said interconnections links layer, said applications layer operating independently of said detecting and re-directing aspects of said interconnection links layer.

28. (New) A module according to claim 5, wherein the module includes:

a power distribution layer;

a clock function layer in communication with the power distribution layer;

switch planes in communication with the clock function layer;

an interconnection links layer for connecting to another interconnection links layer of another of said set of switch modules via at least first and second redundant links, said interconnection links layer for detecting faults in said links and redirecting communication to one of said first and second links whenever faults are detected in the other of said links; and

an applications layer in communication with the interconnection links and providing data packets to said interconnections links layer, said applications layer operating independently of said detecting and re-directing aspects of said interconnection links layer.

29. (New) The method in claim 1, wherein each module includes:

a power distribution layer;

a clock function layer in communication with the power distribution layer;

switch planes in communication with the clock function layer;

an interconnection links layer for connecting to another interconnection links layer of another of said set of switch modules via at least first and second redundant links, said interconnection links layer for detecting faults in said links and redirecting communication to one of said first and second links whenever faults are detected in the other of said links; and

an applications layer in communication with the interconnection links and providing data packets to said interconnections links layer, said applications layer operating independently of said detecting and re-directing aspects of said interconnection links layer.

Respectfully submitted,

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